

SHARED QUEUE FOR MULTIPLE INPUT-STREAMS

BACKGROUND OF THE INVENTION

1. Field of the Invention

5 This invention relates to the field of computer and communications systems, and in particular to a system that receives multiple input-streams that are routed to a common output port.

2. Description of Related Art

10 Multiple-input, common-output systems are common in the art. Multiple hosts, for example, may communicate data to a common server; multiple processors may access a common memory device; multiple data streams may be routed to a common transmission media; and so on. Generally, the input to the multiple-input system is characterized by bursts of activities from one or more input-streams. During these bursts of activities, the arrival rate of input data
15 generally exceeds the allowable departure rate of the data to a subsequent receiving system, and buffering must be provided to prevent a loss of data.

Conventionally, one of two types of systems are employed to manage the routing of multiple input-streams to a common output, dependent upon whether the design priority is maximum memory-utilization efficiency, or maximum performance.

20 In a memory-efficient embodiment, a common buffer is provided for queuing the data from the input-streams, and each process that is providing an input-stream controls access to this common buffer, in accordance with a given control protocol. Data is unloaded from this common buffer to provide the common output. Because a common buffer is used to receive the flow from the various input-streams, the size of the buffer can be optimized for a given
25 aggregate arrival rate. That is, because it is extremely unlikely that all input-streams will be active contemporaneously, the common buffer is sized substantially smaller than the size required to accommodate maximum flow from all streams simultaneously. The performance of such an embodiment, however, is dependent upon the poorest performing process that is providing an input-stream, because a poor process can tie up the common buffer while all of the
30 other processes await access to the common buffer.

To maintain independence among processes that are providing the multiple inputs, conventional high-performance multiple-input systems typically employ multiple input buffers, as illustrated by system 100 of FIG. 1. Each buffer 110 provides a queue for receiving data from its corresponding input-stream 101. In the example of FIG. 1, a receiving system asserts an "Unload(n)" command to select the next-available data-item from the n^{th} queue, and this selected data-item Q_n is subsequently communicated to the receiving system. The selection of the particular input data stream, n , is typically effected based on a prioritization scheme. Not illustrated, the system 100 typically includes a means for notifying the receiving system that data from an input-stream is available, and the receiving system selects from among the available streams based on a priority that is associated with the stream. Alternative protocols for controlling the flow of data from a plurality of input-streams are commonly employed, including, for example, transmission control in the system 100 and a combination of transmission and reception control by the system 100 and the receiving system, respectively. In like manner, the selection of the particular input-stream may include any of a variety of schemes, including a first-in-first-out selection, a round-robin selection, and so on, in addition to, or in lieu of, the aforementioned priority scheme.

The design choices for a multiple-input system include a choice of the size, D , of the input queues. Based on the estimated input and output flow rates, a queue size D can be determined to minimize the likelihood of an overflow of the queue. For ease of understanding, the queues associated with each input-stream 101 of system 100 are illustrated as being similarly sized. If it known that a particular input-stream has a flow rate that substantially differs from the other input-streams, it may be allocated a smaller or larger queue size. As illustrated, the system 100 is configured to allow a maximum burst of D data-items from any of the input-streams, based on the expected processing speed of the subsequent receiving system. Queuing theory techniques are common in the art for determining an optimal value of D , given an expected distribution of arrivals of data-items at any input-stream and an expected distribution of removals of the data-items by the subsequent receiving system.

Because the queue size D is based on estimated arrival rates of data-items from each input-stream, each queue is sized to accommodate a worst-case estimate of arrivals. Although a particular input-stream may frequently come near to filling its queue, the likelihood of all of the input-streams simultaneously coming near to filling all of their queues is generally extremely

low. Viewed another way, the number of unused memory locations among all of the queues at any given time is generally extremely high, and thus the memory-utilization efficiency of the conventional multiple-queue multiple-input system 100 is extremely low.

5

BRIEF SUMMARY OF THE INVENTION

It is an object of this invention to provide a multiple-input device and method that maximizes memory-utilization efficiency. It is a further object of this invention to provide a multiple-input device and method that maximizes memory-utilization efficiency while maintaining a high performance. It is a further object of this invention to provide a high-performance multiple-input device that minimizes the area consumed by memory devices.

10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is explained in further detail, and by way of example, with reference to the accompanying drawings wherein:

FIG. 1 illustrates an example block diagram of a prior art multiple-input queuing system.

5 FIG. 2 illustrates an example block diagram of a multiple-input queuing system in accordance with this invention.

FIG. 3 illustrates an example block diagram of a multiple-input queuing system with a multiple-queue memory-allocation map in accordance with this invention.

10 Throughout the drawings, the same reference numerals indicate similar or corresponding features or functions.

DETAILED DESCRIPTION OF THE INVENTION

15 FIG. 2 illustrates an example block diagram of a multiple-input queuing system 200 in accordance with this invention. The system 200 includes a dual-port memory 220, wherein writes to the memory 220 are controlled by an allocator/arbitrator 240 (hereinafter allocator 240), and reads from the memory 220 are controlled by a mapper/sequencer 250 (hereinafter mapper 250). The write and read processes to and from the memory 220 are symbolically represented by switch 210 and switch 260, respectively.

20 As illustrated in FIG. 2, the memory 220 includes P addressable memory-elements, and each memory-element is of sufficient width W to contain a data-item from any of the input-streams 101. Using conventional queuing theory techniques, the number P of memory-elements required to provide a given level of confidence in avoiding an overflow of the memory 220 can be determined, based on the expected input and output flow rates, as discussed above with regard to the prior art system 100 of FIG. 1. Preferably, the parameter P in system 200 is at least as
25 large as parameter D in system 100. Note, however, that the system 100 includes a total of $N \cdot D$ memory-elements of width W , whereas the memory 220 includes a total of P memory-elements of width W .

30 The allocator 240 is configured to provide the location of a currently-unused memory-element within the memory 220, to which the next data-item from the input-streams 101 is directed, as indicated by output switch S_b in the switch 210. As indicated by the dashed lines between the input-streams 101 and the allocator 240, the allocator 240 is configured to receive a

notification whenever an input-stream 101 has a new data-item to be transmitted. In a preferred embodiment, the allocator 240 includes arbitration logic, in the event that two or more input-streams 101 have data to transmit co-temporaneously. In a straightforward embodiment, for example, the input ports to the switch 210 may be assigned a sequentially ordered priority, the first port being of highest priority, the second port being of lesser priority, and so on. Each input-stream M1, M2, ... MN is physically connected to the particular port depending upon its priority. In such an example, the allocator 240 merely selects, via the input switch Sa, the lowest numbered port that has a data-item to be transmitted. Other priority schemes are common in the art, including dynamic prioritization based on the content of each data-item, or based on a prior history of transmissions from one or more of the input-streams 201, and others. Alternatively, a simple round-robin input selection scheme may be used, wherein the allocator 240 sequentially samples each input-stream 201 for new data, and routes the new data to the next-available unused memory-element in memory 220 in the order in which it is sampled. One of ordinary skill in the art will recognize that the particular scheme used to resolve potential conflicts among the variety of input-streams is independent of the principles of this invention.

Of note, and discussed further below, the allocator 240 is configured to note the removal of data-items from the individual memory-elements. As each data-item is removed, the memory-element that had contained this data-item is now available for receiving new data-items, as a currently-unused memory-element. An overflow of the memory 220 only occurs if all P memory-elements are filled with data-items that have not yet been removed.

Because any input-stream has access to any currently-unused memory-element in the memory 220, the system 100 exhibits the memory-utilization efficiency of the common-buffer system discussed in the Background of The Invention. However, because the allocator 240 is configured to allocate each available memory-element as required, the system 200 is not dependent upon a control of the memory 220 by one or more of the processes that are providing the input-streams.

Further, because the allocation and arbitration functions of the allocator 240, and in particular the allocator's interactions with the switch 210 are substantially independent of the processes that provide the input-streams 101, modifications to the allocator 240 and switch 210 can be effected without requiring changes to the processes that provide the input-streams 101. For example, to improve performance and reduce the likelihood of conflicts among the input-

streams 101, the switch 210 may be configured to allow for the simultaneous routing of multiple data-items to multiple memory-elements in the memory 220. That is, switch Sa is illustrated in FIG. 2 as an N-to-1 switch and switch Sb as a 1-to-P switch. Alternatively, to support up to k simultaneous transfers, switches Sa and Sb may be N-to-k and k-to P switches, respectively.

5 Such a change, however, will be 'transparent' to the input-streams M1... MN, in that the processes that provide the data-items need not be modified to be compatible with an N-to-1 switch, as compared to an N-to-k switch.

10 The mapper 250 is configured to assure that data-items are unloaded/removed from the memory 220 in an appropriate order. If the sequence of output data-items Qn is intended to correspond to the same sequence that the data-items are received, the mapper 250 need merely operate using the same sequence that is applied to control switch Sb in switch 210. That is, for example, if the switch Sb operates to sequentially select memory-elements in memory 220, the mapper 260 would also be configured to sequentially select the memory-elements in memory 220 for communication to a subsequent receiving system. Typically, however, the system 200 is configured to allow the subsequent receiving system to receive data-items in a somewhat independent manner.

15 In a typical embodiment, as discussed above in the Background of the Invention, the receiving system calls for data-items in a sequence that may differ from the sequence in which the data-items are received at the multiple-input queuing system 200. In a preferred embodiment, the system 200 is configured to allow the receiving system to specify the input-stream, n, from which the next data-item is to be sent. In this manner, for example, a process at an input-stream n may initiate a request to send m data-items to the receiving system, and the receiving system subsequently sends m "unload(n)" commands to the queuing system 200 to receive these m data-items, independent of the arrival of other data-items at system 200 from the other input-streams 20 101. That is, relative to each input-stream, the data-items are provided to receiving system in sequence, but the receiving system may call for the data-items from select input-streams independent of the order of arrival of data-items from other input-streams.

25 To allow the receiving system to request a sequence of data-items from a select input-stream, the allocator 240 communicates the allocation of each memory-element location, p, to each input-stream, n, as a stream-element pair (n,p), to the mapper 250. The mapper 250 thereby maintains a list of each memory-element location indicator, p_n, that is sequentially assigned to

each arriving data-item from each input-stream, n . When the receiving system requests the "next" data-item from a particular input-stream, n , the mapper 250 extracts the next location indicator, p_n , from the list associated with the input-stream n , and uses that location indicator p_n to provide the contents of the memory-element p as the output Q_n , via the switch 260. This location indicator p_n is removed from the list associated with the input-stream n , and the allocator 240 thereafter includes the memory-element p as a currently-unused memory location.

FIG. 3 illustrates an example block diagram of a multiple-input queuing system 300 with a multiple-queue memory-allocation map in accordance with this invention, as would be suitable for use as a mapper 250 in the system 200 of FIG. 2. Other embodiments of a mapper 250 will be evident to one of ordinary skill in the art in view of this disclosure.

In the example embodiment of FIG. 3, the mapper 250 includes multiple first-in-first-out (FIFO) queues 355, each queue 355 being associated with a corresponding input-stream 101 to the multiple-input queuing system 300. When the allocator 240 allocates a memory-element p to an input-stream n , the address of this memory-element, p , is stored in the queue corresponding to input-stream n , the index n being used to select the queue 355 corresponding to input-stream n . As each new data-item is received from an input-stream, the address, p , at which the data-item is stored, is stored in the queue corresponding to the input-stream, in sequential order.

Each queue 355 in the example mapper 250 of FIG. 3 is illustrated as having a queue-length of D , consistent with the prior art queue lengths illustrated in FIG. 1. Note, however, that the width of the queues 110 of FIG. 1 is W , so that the total size of each queue 110 is $D \cdot W$. Because each queue 355 of FIG. 3 is configured to store an address to the P memory-elements, the total size of each queue 355 is $D \cdot \log_2 P$. In a typical embodiment, the width of the address, $\log_2 P$ is generally substantially less than the width of a data-item. For example, if the data-items are 32-bits wide, and the buffer 220 is configured to hold 1024 data-items ($\log_2(1024)=10$), the queues 355 of FIG. 3 will be less than a third ($10/32$) of the size of the buffers 110 of FIG. 1.

When the receiving system requests the next data-item from a select input-stream, via an "Unload(n)" command, a multiplexer/selector 350 selects the queue corresponding to the select input-stream, n , and the next available index, p_n , is removed from the select queue 355. The index p_n is used to select the corresponding memory-element p , via that switch/multiplexer 260, to provide the output Q_n corresponding to the Unload(n) request from the receiving system.

After the data-item in the memory-element p is selected for output, the allocator 240 includes the memory-element p as a currently-unused memory-element, thereby allowing it to be allocated to newly arriving data-items, as required.

Also illustrated in FIG. 3 is an example embodiment of a multiple-input, multiple-output, switch 210 that is configured to route a data-item from an input-stream 101 to a selected memory-element, p , in a memory 220. The example switch 210 includes a multiplexer/selector 310 corresponding to each memory-element of the memory 220, that is enabled via a $\text{select}(n_p)$ command from the allocator 240. In this example embodiment, each multiplexer/selector 310 associated with each memory-element is configured to receive a $\text{select}(n_p)$ command, wherein n_p identifies the select input-stream that has been allocated to the memory-element. In this manner, the data-item from the n^{th} input-stream is routed to the p^{th} memory-element. Note that this example embodiment allows for the storage of data-items from multiple co-temporaneous input-streams. That is, for example, if input-streams 1, 3, and 7 are currently attempting to transmit data-items, and memory-elements 2, 8, and 13 (and, perhaps others) are currently-unused, the allocator 240 in a preferred embodiment will assert $\text{select}(1)$, $\text{select}(3)$, and $\text{select}(7)$ commands to the multiplexers 310 that are associated with memory-elements 2, 8, and 13, respectively, thereby simultaneously routing input-stream 1 to memory-element 2, input-stream 3 to memory-element 8, and input-stream 7 to memory-element 13.

Alternative methods for routing data-items from multiple input-streams to allocated memory locations will be evident to one of ordinary skill in the art in view of this disclosure. For example, FIG. 3 illustrates an N-to-1 multiplexer 310 associated with each memory-element of the buffer 220, to select from among N input-streams; in an alternative embodiment, a 1-to-P selector may be associated with each input-stream 101, to route each input-stream to a selected memory-element of the buffer 220.

The foregoing merely illustrates the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements which, although not explicitly described or shown herein, embody the principles of the invention and are thus within the spirit and scope of the following claims.